Birla Institute of Technology & Science, Pilani

Work Integrated Learning Programmes Division
M.S. Software Engineering at Wipro Technologies (WASE)
1st Semester 2015 - 2016
Comprehensive Exam (CDC &Makeup)_ANSWER KEY

Course Number	:	SEWP ZC413
Course Title	:	Computer Organization & Architecture
Type of Exam	:	open book
Weightage	:	60%
Duration	:	3 hrs
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No. of Pages : 3
No. of Questions : 8

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1. Start each answer from a fresh page. All parts of a question should be answered consecutively.
2. Appropriate assumptions can be made and explicitly mentioned .

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1. A computer system has a main memory consisting of 1M 16-bit words. It also has a 4k-word cache organized in the block-set-associative manner, with 4 blocks per set and 64 words per block (6)
   Assume that the cache is initially empty, suppose that the processor fetches 4352 words from location 0,1,2,……..,4351, in that order. It then repeats this fetch sequence nine more times. If the cache is 10 times faster than the main memory estimate the improvement factor resulting from the use of cache. Assume that whenever a block is to be brought from the main memory and the corresponding set in the cache is full, the new block replaces the most recently used block of this set.
   Sol. .After the cache has been filled by the main memory blocks 0, 1, _ _ _, 63 on the first pass, block 64 replaces block 48 in set 0. On the second pass, block 48 replaces block 32 in set 0. On the third pass, block 32 replaces block 16, and on the fourth pass, block 16 replaces block 0. On the fourth pass, there are two replacements: 0 kicks out 64, and 64 kicks out 48. On the sixth, seventh, and eighth passes, there is only one replacement in set 0. On the ninth pass there aretwo replacements in set 0, and on the final pass there is one replacement. The situation is similar in sets 1, 2, and 3. Again, there is no contention in sets 4 through 15. In total, there are 11 replacements in set 0 in passes 2 through 10. The same is true in sets 1, 2, and 3. Therefore, the improvement factor is

   Improvement factor = Time without cache /Time with cache
   $=10 \times 68 \times 10\tau / 1 \times 68 \times 11\tau + 4 \times 11 \times 11\tau + (9 \times 68-44) \times 1\tau = 3.78$

2. Assume that for a computer with 8085 CPU, we have to interface a direct mapped cache memory and a cache controller. Assume that 8085 is interfaced with 64kB of memory through 16 address lines and 8 data lines. This 64kB is divided into 128 pages of 512 bytes each. Each page is sub divided to 64 sets of 8 lines each. Each line is composed of only one byte. Calculate the size of cache and the width and size of cache directory necessary for the system. (4)
   As each page of main memory is of 512 bytes same would be the size of cache.

A2-A0 to target any line 1 to 8, A8-A3 to target 1 of 64 sets and A15-A9 to target available pages of main memory.
The cache directory must have 64 rows one each for possible 64 sets. In each row most significant 7 bits used as tag address , one bit as the tag valid bit. To indicate validity of 8 lines of the set there must be another 8 bits within the same row in cache directory. Therefore every row of cache directory would need 16 bits. Therfore the width of cache directory would be 16-bits and it must contain 64 rows.

3. a. During an instruction, if there are 24 sequence counter inputs in a hardwired encoder and it is driven by 1 GHz clock, then what will be the maximum time taken to process an instruction? (2)

   Sol. Maximum number of states for an instruction = 24. Hence the maximum time shall be 24ns

   b. During an instruction, there are 16 microinstructions in control store memory that generate the control signals . if it takes 5 microinstructions to read an instruction from memory into instruction register IR and then to decode the instruction, what will be the time taken by the processor for the instruction? Assume a read of control memory address occurs in 1 ns. (2)

   Sol: Hence time required is (5 + 16) X 1 ns= 21ns

4. The average seek time and rotational delay in a disk system are 6ms and 3ms respectively. The rate of data transfer to or from the disk is 30Mbytes/sec and all disk accesses are for 8 kBytes of data. Disk DMA controllers, the processor, and the main memory are all attached to a single bus. The bus data width is 32 bits, and a bus transfer to or from the main memory takes 10 ns.

   a. What is the maximum number of disk units that can be simultaneously transferring data to or from the main memory? (4)

   Sol: The rate of transfer to or from any one disk is 30 megabytes per second. Maximum memory transfer rate is $4/(10 \times 10^{-9}) = 400 \times 10^{6}$ bytes/s, which is 400 Mega bytes per second. Therefore, 13 disks can be simultaneously flowing data to/from the main memory.

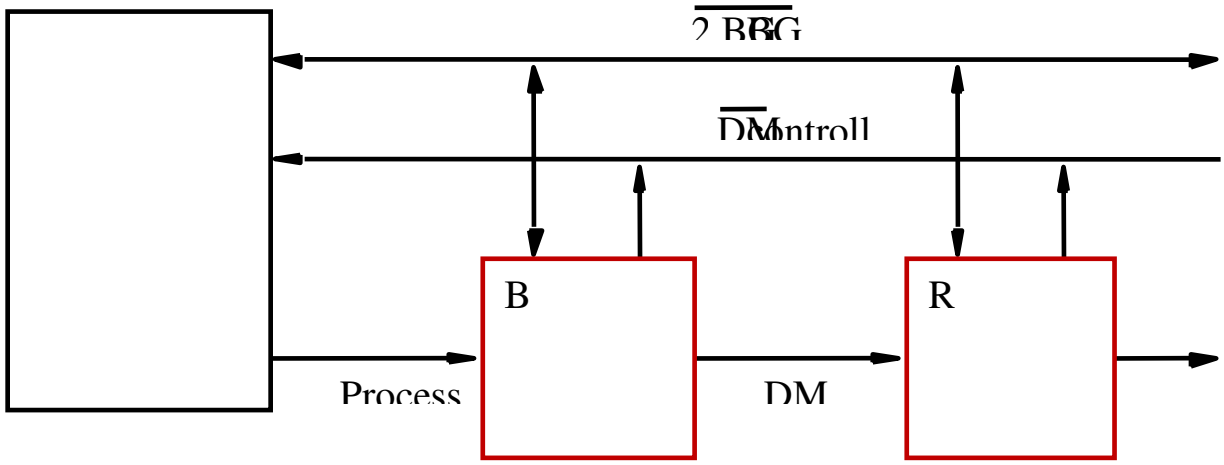
   b. What percentage of main memory cycles are stolen by a disk unit. On average, over a long period of time during which a sequence of independent 8k-byte transfers take place? (3)

   Sol: 8K/30M = 0.27 ms is needed to transfer 8K bytes to/from the disk. Seek and rotational delays are 6 ms and 3 ms, respectively. Therefore, 8K/4 = 2K words are transferred in 9.27 ms. But in 9.27 ms there are $(9.27 \times 10^{-3})/(0.01 \times 10^{-6}) = 927 \times 10^{3}$ memory (word) cycles available. Therefore, over a long period of time, any one disk steals only $(2/927) \times 100 = 0.2\%$ of available memory cycles.

5. Assume that the bus arbitration arrangement shown in figure, the processor keeps asserting BG1 as long as $\overline{BR}$ is asserted. When device d is requesting the bus, it becomes the bus master only when it receives a low to high transition on its BG_d input. (4)

a. Assume that devices are allowed to assert the BR signal at any time. Give the sequence of events to show that the system can enter a deadlock situation, in which one or more devices are requesting the bus, the bus is free, and no device can become the bus master

b. Suggest a rule for the devices to observe in order to prevent this deadlock situation from occurring. (3)



Sol:

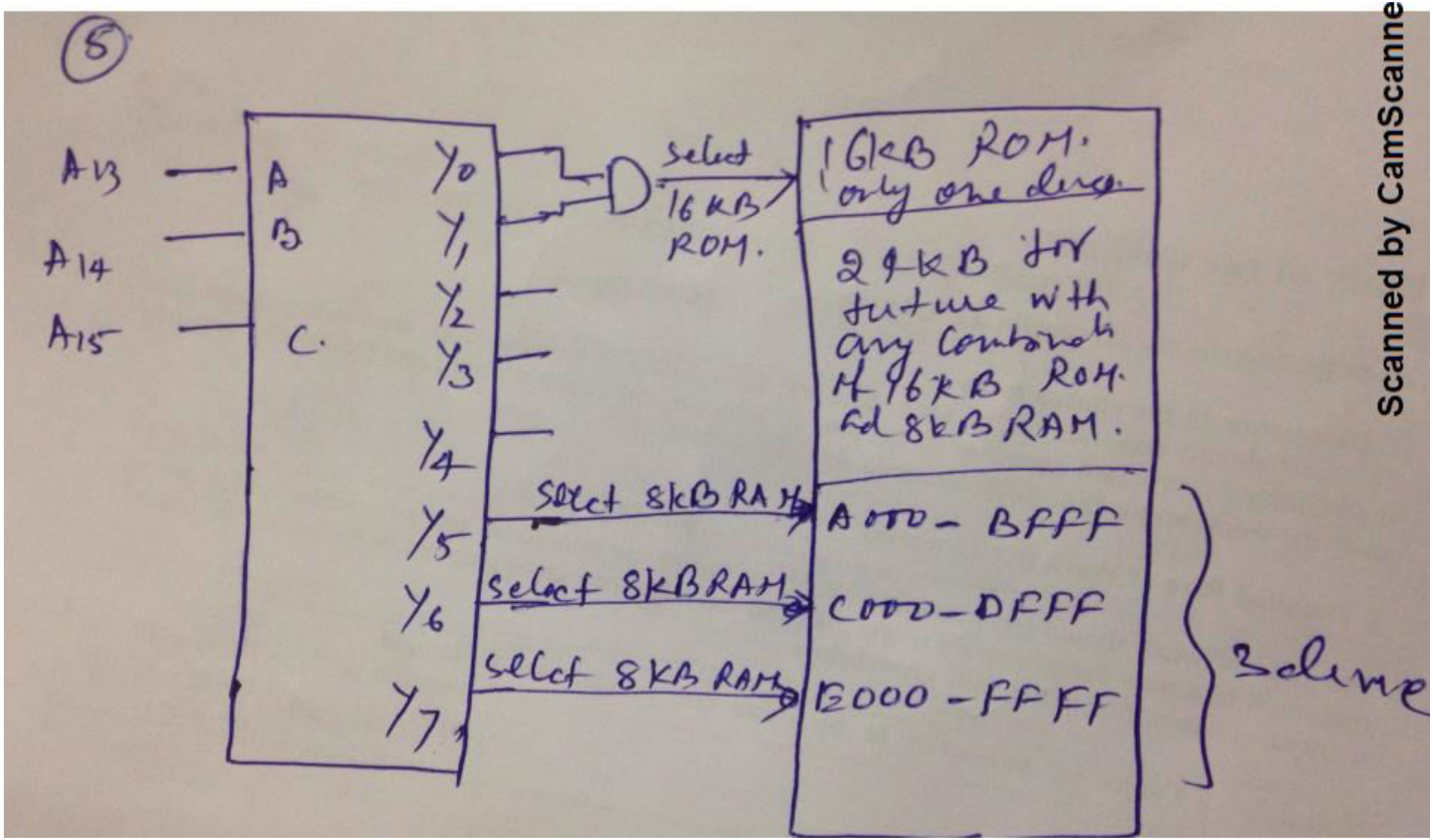
(*a*) Device 2 requests the bus and receives a grant. Before it releases the bus, device 1 also asserts BR. When device 2 is finished nothing will happen. BR and BG1 remain active, but since device 1 does not see a transition on BG1 it cannot become the bus master.

(*b*) No device may assert BR if its BG input is active.

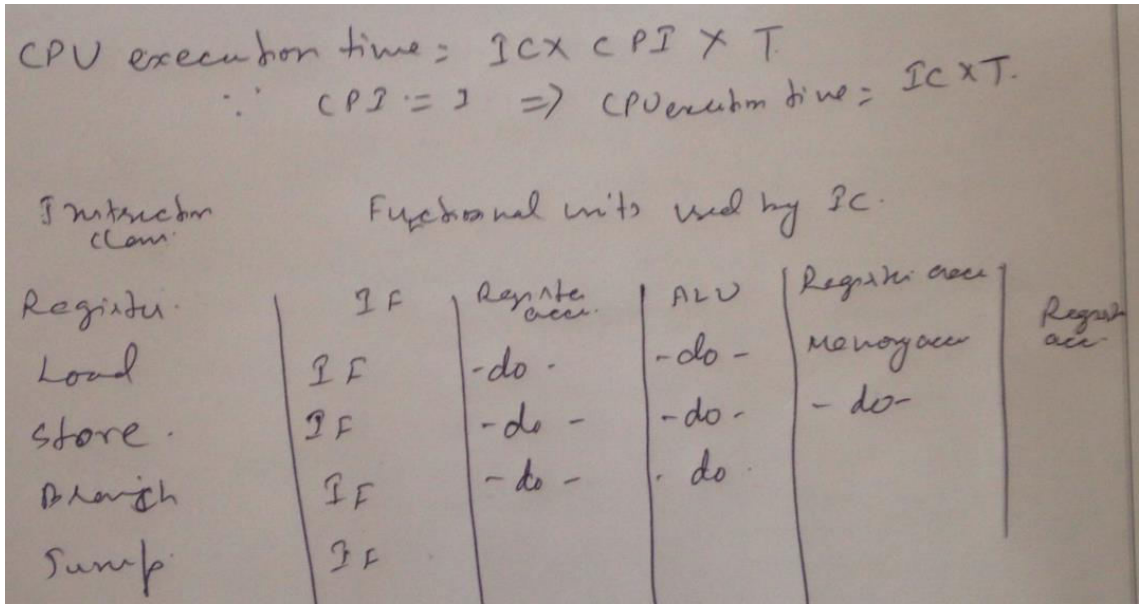
6. Let us assume that a processor can address a maximum of 64kB memory area for which the memory devices are to be a combination of RAM and ROM. The requirement of ROM is 16kB, which must be continuous starting from the lowest addressable memory space. The system also demands 24kB of RAM at the highest memory address. The remaining part of addressable memory space is left for future expansion, which may contain any combination of RAM and ROM. If ROM devices of 16kB capacity and RAM ICs of 8kByte capacity are available to the designer, then how the memory decoding is to be completed? 10

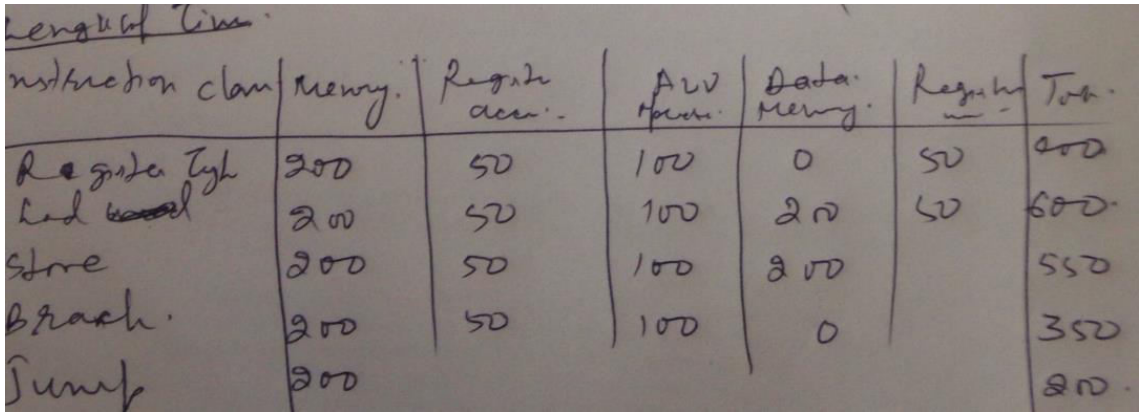
Soln

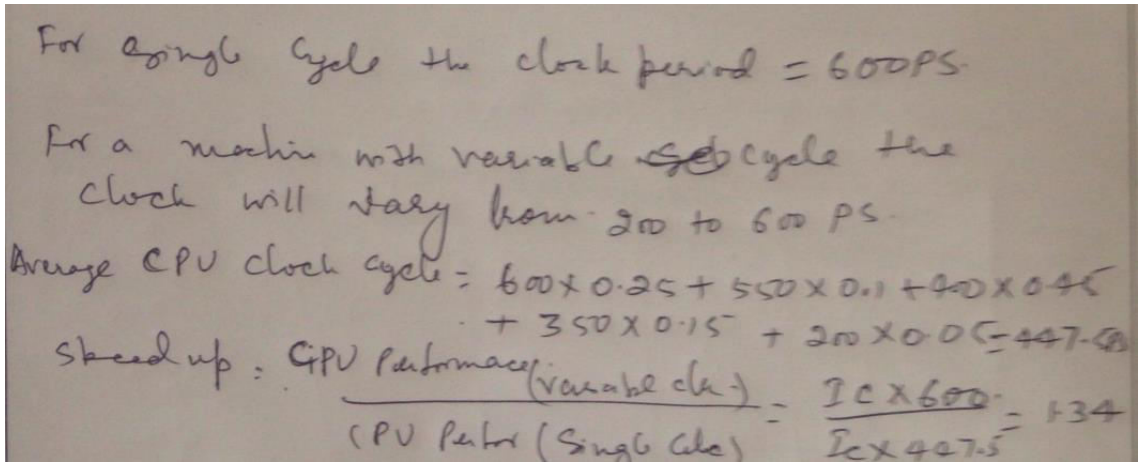
(5)



7. Assume that the operation times for the major functional units in this implementation are the following:
   Memory units: 200 ps; ALU and adders: 100ps; Register file (read or write): 50ps
   And assume the following instruction mix 25 % load, 10 stores,45% ALU instructions, 15% branches and 5% jump
   Other hardware components have no delays
   Which of the following implementation will be faster and by how much?
   An implementation in which every instruction operates in 1 clock cycle of a fixed length or an implementation in which every instruction executes in 1 clock cycle using a varying length clock, which for each instruction is only as long as it needs to be.
   SOL







8. Write a program to evaluate the arithmetic statement using ONE address Instruction

$$P = \frac{(X - Y + Z) * (M * n - o)}{Q + R * S}$$ (5)

Sol

LOAD	X	AC ← M [X]
ADD Z		AC ← AC + M[Z]
SUB Y		AC ← AC - M[Y]
STORE	T	M [T] ← AC
LOAD	M	AC ← M[m]
MUL	N	AC ← AC x M[n]
SUB	O	AC ← AC – M[o)
MUL	T	AC ← AC x M[T]
STORE	U	M[U] ← AC
LOAD	R	AC ← M [R]
MUL	S	AC ← AC x M[S)
ADD	Q	AC ← AC + M [Q]
DIV	V	AC ← M[v]/ AC
STORE	P	M[P] ← AC

9. A Computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part.

(i) How many bits are there in the operation code, the register code part and the address part?

(ii) Draw the instruction word format and indicate the number of bits in each part.

(iii) How many bits are there in the data and address inputs of the memory?

Ans.

(i) For a memory unit with 256K words of 32 bits each we need 18 bits to specify an address.

Operation Code =
7 bits
32-25 = 7 bits for
opcode Register
Code = 6 bits
$> 2^6 = 64$

(ii) Instruction Word Format

	1	7	6	18 = 32 bits
	I	Opcode	Register Code	Address

(iii) data and address inputs of the memory data = 32 bits
address = 18 bits

10. How many characters per second can be transmitted over a 1200 baud line in asynchronous serial transmission in following modes – assume a character code is of eight bits? (1+1+1)

(i) Synchronous Serial transfer

(ii) Asynchronous Serial Transfer with 2 stop bits

(iii)Asynchronous Serial Transfer with one stop bit

Sol: Baud Rate = 1200
Character Code = 8 bits
(i) Transmitted Characters per second in Synchronous Serial transmission
Transfer = 1200/8=150 Character per second
(ii) Asynchronous Serial Transfer with 2 stop bits
total number of bits = 1 start bit + 8 information bits + 2 stop bits
= 1+8+2 = 11 bits
baud rate = 1200
Transmitted Character per second = 1200/11= 109 Character per second
(iii) Asynchronous Serial Transfer with one stop bit.
Total no. of bits = 1 start bit + 8 information bits + 1 stop bit = 10 bits
band rate = 1200
Transmitted Character per second = 1200/10 = 120 Character per second