# Birla Institute of Technology \& Science, Pilani <br> Work Integrated Learning Programmes Division M.S. Software Engineering at Wipro Technologies (WASE) <br> $1^{\text {st }}$ Semester 2015-2016 <br> Comprehensive Exam ( Regular )_ANSWER KEY 

| Course Number | SEWP ZC413 |  |
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| Course Title | Computer Organization \& Architecture | No. of Pages: 3 <br> No. of Questions: 7 |
| Type of Exam | open book |  |
| Weightage | 60\% |  |
| Duration | 3 hrs |  |
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1. A computer system has a main memory consisting of 1 M 16 -bit words. It also has a 4 k -word cache organized in the block-set-associative manner, with 4 blocks per set and 64 words per block
a. Calculate the number of bits in each of the TAG, SET, and WORD fields of the main memory address format
b. Assume that the cache is initially empty, suppose that the processor fetches 4352 words from location 0,1,2 $\qquad$ .,4351, in that order. It then repeats this fetch sequence nine more times. If the cache is 10 times faster than the main memory estimate the improvement factor resulting from the use of cache. Assume that the LRU algorithm is used for block replacement. Sol:
(a) TAG field is 10 bits. SET field is 4 bits. WORD field is 6 bits.
(b) Words $0,1,2, \ldots, \quad 4351$ occupy blocks 0 to 67 in the main memory (MM). After blocks 0, 1, $2, \ldots, 63$ have been read from MM into the cache on the first pass, the cache is full. Because of the fact that the replacement algorithm is LRU, MM blocks that occupy the first four sets of the 16 cache sets are always overwritten before they can be used on a successive pass. In particular, MM blocks $0,16,32,48$, and 64 continually displace each other in competing for the 4 block positions in cache set 0 . The same thing occurs in cache set 1 ( MM blocks, $1,17,33,49$, 65 ), cache set 2 ( MM blocks $2,18,34,50,66$ ) and cache set 3 ( MM blocks $3,19,35,51,67$ ). MM blocks that occupy the last 12 sets (sets 4 through 15) are fetched once on the first pass and remain in the cache for the next 9 passes. On the first pass, all 68 blocks of the loop must be fetched from the MM. On each of the 9 successive passes, blocks in the last 12 sets of the cache ( $4 \times 12=48$ ) are found in the cache, and the remaining $20(68-48)$ blocks must be fetched from the MM .

Improvement factor $=$ Time without cache /Time with cache

$$
=10 \times 68 \times 10 \mathrm{~T} / 1 \times 68 \times 11 \mathrm{t}+9(20 \times 11 \mathrm{t}+48 \text { X 1т })=2: 15
$$

2. A processor has 24 distinct instructions with 12 instructions having 8 microinstructions and 12 having 16 microinstructions
a. How many addresses are used in control store memory?
b. If four instructions branch to another set of microinstructions, each having four instructions, then how many addresses are now used in control store memory? Assume that each microinstruction also stores a branch address and thus neglect branching microinstructions

Sol a. number of addresses $=12 \times 8+12 \times 16=288$
b. Number of addresses $=12 \times 8+12 \times 16+4 \mathrm{X} 4=304$
3. A disk unit has 24 recording surfaces. It has a total of 14,000 cylinders. There is an average of 400 sectors per track. Each sector contains 512 bytes of data.
a. What is the maximum number of bytes that can be stored in this unit?

Sol: The maximum number of bytes that can be stored on this disk is 24 X14000 X $400 \times 512=68.8$ $\mathrm{X} 10^{9}$ bytes.
b. What is the data transfer rate in bytes per second at a rotational speed of 7200rpm Sol: The data transfer rate is $(400 \times 512 \times 7200) / 60=24: 58 \times 10^{6}$ bytes/s.
c. Using a 32 bit word, suggest a suitable scheme for specifying the disk address, assuming that there are 512 bytes per sector.
Sol: Need 9 bits to identify a sector, 14 bits for a track, and 5 bits for a surface. Thus, a possible scheme is to use address bits A8-0 for sector, $\mathrm{A}_{22-9}$ for track, and $\mathrm{A}_{27-23}$ for surface identification. Bits $\mathrm{A}_{31-28}$ are not used.
4. a.In the arrangement in figure below, a device becomes the bus master only when it receives a low to high transition on its bus grant input. Assume that device 1 requests the bus and receives a grant. While it is still using the bus, device 3 asserts its BR output. Draw a timing diagram showing how device 3 becomes the bus master after device 1 releases the bus.

Sol 4 (a)

b.Write a program to evaluate the arithmetic statement using Zero address Instruction

$$
\begin{equation*}
P=\frac{(X-Y+Z) *(M * n-o)}{Q+R * S} \tag{5}
\end{equation*}
$$

| PUSH X |  | TOS $\leftarrow \mathrm{X}$ |
| :--- | :--- | :--- |
| PUSH Y |  | TOS $\leftarrow \mathrm{Y}$ |
| SUB |  | TOS $\leftarrow \mathrm{X}-\mathrm{Y}$ |
| PUSH | Z | TOS $\leftarrow \mathrm{Z}$ |
| ADD |  | TOS $\leftarrow(\mathrm{X}-\mathrm{Y}+\mathrm{Z})$ |
| PUSH | M | TOS $\leftarrow \mathrm{M}$ |
| PUSH | N | TOS $\leftarrow \mathrm{N}$ |
| MUL |  | TOS $\leftarrow \mathrm{M} * \mathrm{~N}$ |
| PUSH | O | TOS $\leftarrow \mathrm{O}$ |
| SUB |  | TOS $\leftarrow\left(\mathrm{M}^{*} \mathrm{~N}-\mathrm{O}\right)$ |
| MUL |  | TOS $\leftarrow(\mathrm{X}-\mathrm{Y}+\mathrm{Z}) \mathrm{x}$ <br> $(\mathrm{M} * \mathrm{~N}-\mathrm{O})$ |
| PUSH | R |  |
| PUSH | S | TOS $\leftarrow \mathrm{R}$ |
| MUL |  | TOS $\leftarrow \mathrm{S}$ |
| PUSH | Q | TOS $\leftarrow \mathrm{R} \leftarrow \mathrm{Q}$ |
| ADD |  | TOS $\leftarrow \mathrm{Q}-\mathrm{R} * \mathrm{~S}$ |
| DIV | O |  |
| POP | P | $\mathrm{M}[\mathrm{P}] \leftarrow \mathrm{TOS}$ |

5. Suppose we have a 6 stage pipelining. When we run a program of 100 lines of instructions, suppose there have been 20 instructions which have 1 stall cycle. What would be the CPI in this execution? Be sure to count the exact number of clock cycles used
Sol. Execution time $=100+(6-1)+20=125$ cycles; $\mathrm{CPI}=125 / 100=1.25$
6. Design the data path of a processor so that it can complete the execution of return from subroutine instruction within five cycles.
Sol

| step | Single bus system(only c- <br> bus) | For two bus system(c-bus and B-bus) |
| :--- | :--- | :--- |
| 1 | Copy PC to MAR | Copy PC to MAR through B-Bus, Copy SP to Y of <br> ALU using C-Bus |
| 2 | Output MAR to get opcode <br> byte in MBR | Output MAR to external Mamory bus and get <br> opcode byte in MBR. Increment ALU by one and <br> store result in Z |
| 3 | Copy MBR to IR and <br> instruction decode | Copy MBR to IR through B-bus and instruction <br> decode, Copy Z back to SP and MAR through C- <br> bus |
| 4 | Copy SP to ALU and <br> increment it by one | Output MAR to external Memory bus to get <br> return address in MBR |
| 5 | Copy Z back to SP and MAR | Copy MBR to PC using B-bus |
| 6 | Output MAR to get return <br> address in MBR |  |
| 7 | Copy MBR to PC |  |

7. Suppose we have a floating-point unit that requires 400 ps for a floating-point add and 600 ps for a floating-point multiply, not including the time to get the instruction or read and write any registers, which take the same as for an integer. Assume that the operation times for the major functional units in this implementation are the following:
Memory units: 200 ps; ALU and adders: 100ps; Register file (read or write): 50ps
All loads take the same time and comprise $30 \%$ of the instructions. All stores take the same time and comprise $15 \%$ of the instructions. R-format instructions comprise $25 \%$ of the mix. Branches comprise $10 \%$ of the instructions, while jumps comprise $5 \%$. FP add and subtract take the same time and together total $5 \%$ of the instructions. FP multiply and divide take the same time and together total $10 \%$ of the instructions.
Other hardware components have no delays
Which of the following implementation will be faster and by how much?
An implementation in which every instruction operates in 1 clock cycle of a fixed length or an implementation in which every instruction executes in 1 clock cycle using a varying length clock, which for each instruction is only as long as it needs to be.

Uexecuthor time $=I C \times C P I \times 1$
$\because C P I=3 \Rightarrow C P$ Uesestm tive $=I C \times T$.
Find cqel clock $=100$, studut $=\frac{900}{545.5}=1.66$
Initretor Fuctramel units we hy $3 C$


8. Show the memory organization (1024 bytes) of a computer with four 128x8 RAM Chips and $512 x 8$ ROM Chip. How many address lines are required to access memory

Pls consider 128 X 8 ROM as 512 X 8 in the solution


